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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/872,796	06/01/2001	Craig L. Stevens	10001.000600 (NVLS 379)	4156

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OKAMOTO & BENEDICTO, LLP
P.O. BOX 641330
SAN JOSE, CA 95164

EXAMINER	
KIELIN, ERIK J	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 09/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/872,796	STEVENS ET AL.	
	Examin r	Art Unit	
	Erik Kielin	2813	

-- The MAILING DATE of this communication appears on th cover sh t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-13,17 and 19-21* is/are pending in the application.

4a) Of the above claim(s) *none* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-13,17 and 19-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *19* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11 August 2003 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims **1**-7, 9-13 and **17**, 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,251,759 B1 (**Guo** et al.) in view of US 5,281,320 (**Turner** et al.) and US 6,270,582 B1 (**Rivkin** et al.).

Regarding independent claims 1 and 17, **Guo** discloses a wafer processing system comprising:

a load lock **114** (Fig. 1);

a transport module having a load chamber **113** (called "buffer chamber" in Guo), a transfer chamber **101**, and a pass-through chamber **122** (additionally called "transition chambers"

in Guo col. 4, line 19) located between the load chamber and the transfer chamber, the load chamber being coupled to the load lock;

an intermediate process module **124** (called "transition chambers" in Guo col. 4, line 19) coupled to the load chamber and the transfer chamber (as further limited by instant claim 20);

a first set of process modules **116, 118, 121** coupled to the load chamber;

a second set of process modules **104, 106, 108, 110** coupled to the transfer chamber.

Guo does not indicate if the load lock is a single-wafer load lock having only one pedestal configured to support a single wafer thereon.

Turner teaches a single wafer load lock chamber **12** (Figs. 4-6) having only one pedestal **60** (called a "vacuum chuck" at col. 12, line 20) configured to support a single wafer **15** thereon in a cluster tool (Figs. 1-2). Turner teaches that the benefit of load lock is that the volume is minimized to accommodate a single wafer in order to reduce the amount of pumpdown required for the load lock (col. 7, lines 12-16; col. 10, lines 24-39).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use a single-wafer load-lock having only one pedestal configured to support a single wafer thereon as the load lock in Guo, in order to reduce the amount of pumpdown required for the load lock and thereby increase wafer processing throughput, as taught by Turner.

Then the only difference is that neither **Guo** nor **Turner** teaches that the single-wafer load-lock has an integral cooling unit for cooling the single wafer.

Rivkin teaches a single-wafer load lock (title) for a multi-chamber semiconductor wafer process module having water-cooled, single-wafer pedestal **136**, wherein the cooling unit is integrally formed with the pedestal and the load lock chamber and uses water cooling to cool the

single wafer --as further limited by instant claim 19 (Fig. 3; col. 6, lines 1-4, lines 37-47). **Rivkin**, like **Turner**, recognizes that the volume of the load lock should be minimized to increase throughput (col. 4, lines 25-29). **Rivkin** also teaches that preprocessing by pre-heating or cooling the single wafer increases the efficiency of processing throughput (col. 3, lines 18-36).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to incorporate integral cooling into the load lock of **Turner** in order to perform preprocessing on the wafer and thereby increase processing throughput, as taught by **Rivkin**.

Regarding claims 2, **Guo** shows process module **118** connected to the load chamber 113 (the first set of process modules) may be a pre-clean module (col. 4, line 7).

Regarding claims 3 and 4, **Guo** shows process module **121** connected to the load chamber 113 (the first set of process modules) may be a physical vapor deposition (PVD) or chemical vapor deposition (CVD) module (col. 4, lines 49-52).

Regarding claim 6, **Guo** shows process module **104** connected to the transfer chamber 101 (the second set of process modules) is a chemical vapor deposition (CVD) module (col. 4, lines 64-66).

Regarding claims 10, 11, and 21, **Guo** discloses that it is known for the intermediate process module **122** to be configured as either a cooling station or a pre-clean module (col. 1, 45-48; col. 4, line 47).

Regarding claim 12, **Guo** shows the intermediate process module **124** is configured as a PVD chamber.

Regarding claims 5, 7, 9, and 13, **Guo** does not specifically indicate that the second set of process modules (those on the transfer chamber **101**) include a pre-clean module (claim 5) or a

PVD module (claim 7), or that the intermediate process module **122**, **124** may be configured as a degas module (claim 9) or a CVD module (claim 13). Note however, that **Guo** teaches the benefits of configuring one of the intermediate chambers **122**, **124** as a PVD module (col. 3, lines 43-50). Additionally, **Guo** teaches that the ordering of process modules is "illustrative" (col. 3, lines 60-63), and that cluster tools include a variety of ordered tools depending upon the process being performed (col. 1, lines 30-48), and also that metallization cluster tools include CVD, PVD, pre-clean and degas modules, among others (col. 2, lines 34-59 and through out the specification and figures). This suggests to one of ordinary skill in the art that the arrangement is a matter of design choice to best suit a given processing steps to be performed in a semiconductor wafer. Moreover, it has been held that mere rearrangement of parts is evidence of obviousness. *In re Kuhle*, 526 F.2d 553, 188 USPQ 7 (CCPA 1975) (the particular placement of a contact in a conductivity measuring device was held to be an obvious matter of design choice).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to have a pre-clean module or PVD module in the second set of process modules and to have a degas and pre-clean modules as intermediate modules, in order to optimize the process throughput for a given process, as taught by **Guo** and according to precedent. Moreover, Applicant indicates that virtually any arrangement of process modules is possible, thereby teaching away from the criticality of any specific arrangement in the processing system.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed.

Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims **1**-7, 9-13 and **17**, 19-21 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 2 of U.S. Patent No. 6,431,807 B1 (**Stevens** et al.) in view of US 6,251,759 B1 (**Guo** et al.).

Claims 1 and 2 of the Stevens patent claim a single-wafer load lock having only one pedestal configured to support a single wafer thereon, wherein the load-lock has an integral cooling unit to cool the single wafer and a transfer chamber and liquid cooling.

Guo teaches a wafer processing system having the remaining features of the claims, as explained above.

It would have been obvious for one of ordinary skill in the art, at the time of the invention to incorporate the cluster system of **Guo** into the single-wafer system of **Stevens**, in order to form the cluster tool having high throughput, as taught by **Guo**.

Response to Arguments

6. Applicant's arguments with respect to all pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 703-306-5980. The examiner can normally be reached on 9:00 - 19:30 on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 703-308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Erik Kielin
Primary Examiner
September 10, 2003